receiving a residual time stamp that represents a modulo 2^P value of a number of network clock cycles in a time interval defined by a fixed number of timing clock cycles of the service input signal, wherein 2^P represents a range of possible deviations in the number of network clock cycles within the time interval;

determining, from the residual time stamp and the network clock cycles, the time interval; and

recovering the timing clock of the service input signal based on the determined time interval and the fixed number of timing clock cycles.--

B1 Cont.

REMARKS

This Preliminary Amendment addresses issues raised in the Office Action dated December 30, 1998, in the parent application of this Rule 53(b) Continuation Application. In the Office Action, the Examiner rejected claims 34-37 under 35 U.S.C. §103(a) as being unpatentable over Ishikawa (JP 3-114333) in view of CCITT Study GroupXVIII/8 entitled "Proposed method to provide the clock recovery function for circuit emulation" (hereinafter "Matsuyama"). Claims 34-37 of the parent application appear in the present Continuation Application as new claims 33-36.

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Applicants have canceled claims 1-10 and 12-32, and added 33-36 claims to expedite prosecution of the parent application. Claim 11 has been retained for the purpose of filing this continuation reissue application. Claims 11 and 33-36 remain in the application.

Applicants respectfully disagree with the Examiner's rejections in the December 30, 1998 Office Action. On March 23, 1999, an interview was conducted with Examiner Vo to discuss the differences between the present invention and the references cited by the Examiner. At this interview Applicants agreed to provide a response, and Examiner Vo agreed to reconsider his rejections.

Ishiwaka, the primary reference cited by the Examiner discloses a clock synchronization format in which the transmitter transmits, in the form of packets, transmitter clock frequency data indicating the relative frequency of the transmitting clock. The receiver then compares a receiver clock frequency with the received transmitter clock frequency in order to synchronize the transmitter clock and receiver clock. Ishikawa does not address the question of how to transmit time stamp information like the present invention.

Matsuyama, the secondary reference relied on by the Examiner, does address time stamping, but merely discloses a time stamping technique in which reference

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timing is used to increment a modulo 2^{16} counter (16 bits) at the transmitter. This reference timing is derived from the either the timing of the physical interface or from the reception of a clock cell and is disclosed as the network reference timing. Every 16 cells the contents of this counter is read out and transferred to the receiver. This value is called the Time Stamp (TS), indicates the time this cell entered the ATM network, and requires a 16 bit cell to transmit the information.

In contrast, the present invention as recited in independent claims 33 and 35 recites determining or receiving a modulo 2^p value, wherein 2^p represents a range of tolerance in the timing clock of the service input. As described above, the 2^{16} counter disclosed in Matsuyama is used to determine the actual number of clock cycles during the time stamp period, and as such 2^{16} does not represent a range of tolerance in the timing clock.

As such, Matsuyama does not teach or suggest determining a modulo 2^p value, wherein 2^p represents a range of tolerance in the timing clock of the service input signal, as recited in new claims 33 and 35.

With regard to independent new claims 34 and 36, as described above, the 2^{16} counter disclosed in Matsuyama is used to determine the actual number of clock cycles during the time stamp period. In contrast, independent claims recite a determining a modulo 2^p value, wherein 2^p represents a range of possible deviations in the number of

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network clock cycles within each of the time intervals. Thus, the 2^{16} counter disclosed in Matsuyama does not represent a range of possible deviations in the number of clock cycles within each time interval, but instead represents the actual number of clock cycles in the time interval.

Accordingly, Applicants submit that neither Iwata nor Matsuyama taken alone or in combination, disclose or suggest the combination of elements as recited in claims 33-36.

For at least the foregoing reasons, Applicants submit that independent claims 33-36 are allowable over Iwata and Matsuyama.

Respectfully submitted,

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